AMENDMENTS TO THE SPECIFICATION

[0001] ~~The~~ Embodiment of the present invention relate ~~relates~~ generally to computer processor power management[[,]] and, more ~~specifically~~ particularly, to an improved method for determining optimum performance level transition points.

[0004] More recent systems address this concern by taking advantage of the equation governing power consumption in CMOS circuits. This equation is $P=kV^2F$, where P is the power consumed, k is some constant, V is the applied voltage and F is the operating frequency. Application of this equation shows that a small reduction in voltage may provide a large reduction in power consumption. Using a voltage-varying scheme in which the power is applied over time, therefore, allows for fixed workload to be accomplished with less energy and hence prolonged battery life. A typical PMS would provide a high-voltage/high-frequency mode for AC use and a low-voltage/low-frequency mode for DC use. The modes are implemented by a software program which detects whether the AC adapter has been plugged in, or not, and switches mode accordingly. The user could also provide input to the system and, if desired, choose ~~chose~~ not to switch to low performance mode. The PMS software may be incorporated within the OS and indicates to an application and driver that the power source has changed, the driver then communicates with the firmware that switches modes.

[0006] ~~The~~ Embodiment of the present invention are ~~is~~ illustrated by way of example and not intended to be limited by the figures of the accompanying drawings in which like references indicate similar elements and in which:

[0007] **Figure 1** illustrates ~~is a diagram illustrating~~ a computing system for implementing one embodiment of the present invention;

[0008] **Figure 2** illustrates an embodiment of processor utilization graphs ~~is a block diagram of a power control circuit for implementing the present invention~~; and

[0009] **Figure 3** illustrates an embodiment of a process for calculating processor utilization ~~depicts typical processor utilization graphs~~.

[0011] **Figure. 1** is a diagram illustrating an exemplary computer system 100 for implementing one embodiment of the present invention. The sampling of processor utilization, the detection of a change in processor utilization, and the transition of the processor to a different performance level, described herein, may be implemented and utilized within computing system 100. Computing system 100 may represent a general-purpose computer, portable computer, or other like device. The components of computing system 100 are exemplary in which one or more components may be omitted or added.

[0020] In accordance with one embodiment of the present invention, processor utilization is measured every T seconds. The processor-utilization monitoring period, T, should be small enough so that increased processor utilization is detected quickly, this maintains the responsiveness of the system. T should not be so small, however, as to overly tax the processor resources. When processor utilization is detected above a given threshold the system is automatically switched to a higher performance level. When processor utilization is detected below a given threshold the system is automatically switched to a lower performance level. Frequent switching between higher and lower performance levels taxes the processor, therefore

the FUSD transition policy allows for less frequent switching from a high performance level to a lower one so that quick reversals in processor utilization will not result in frequent switching. For example, as shown in Figure 2b the processor utilization reaches a switch-up threshold of, for example, 95% at time T_1. The system automatically transitions to a higher performance level. At time T_2 the processor utilization drops below a switch-down threshold, for example 75%, but the system does not transition to a lower performance level. Instead, current performance level is maintained until processor utilization is monitored at time T_3. At time T_3 the processor utilization is again above the switch-up threshold so the higher performance level is maintained. When, at time T_4-T_6 the processor utilization level remains below the switch-down threshold for 3T seconds, the system is then transitioned to a lower performance level. The system remains at this lower performance level until the processor utilization once again rises above the switch-up threshold (i.e., until time T_9).